WHAT IS CLAIMED IS:

1. A clock ride-over circuit in which an input digital signal synchronized with a first clock signal is converted into a digital signal synchronized with a second clock signal, and in which a result of conversion is output as an output digital signal, comprising:

(a) a first synchronization circuit matching a phase of an input digital signal to a phase of said first clock signal to output said input digital signal phase-matched to said first clock signal;

(b) a selector selecting said input digital signal phase-matched to said first clock signal or an output digital signal of the check ride-over circuit, depending on a value of a selection signal of the same frequency as that of said first clock signal, to output a selected digital signal as an intermediate digital signal;

(c) a second synchronization circuit synchronizing said intermediate digital signal to output said intermediate digital signal synchronized with said second clock signal as said output digital signal; and

(d) a timing control circuit generating said selection signal based on said first clock signal and said second clock signal.

2. The clock ride-over circuit as defined in claim 1 wherein said timing control circuit comprises:

(d1) a clock detection unit detecting the phase of the first

clock signal to output a detected result as a detection signal;

(d2) a self-running counter outputting said selection signal using said second clock signal as a clock signal; and

(d3) a phase comparator comparing the phase of said detection signal to that of said selection signal to reset the phase of said self-running counter if the phase difference therebetween is outside an allowable range.

3. The clock ride-over circuit as defined in claim 2 wherein said allowable range begins with a timing at which said first clock signal changes and continues a plurality of periods of said second clock signal, said self-running counter outputting said selection signal at a trailing end of said allowable range after resetting.

4. The clock ride-over circuit as defined in claim 1, wherein said second clock signal has a higher speed than said first clock signal.

5. The clock ride-over circuit as defined in claim 3, wherein said plurality of periods include at least 2 or 3 periods of said second clock signal.

6. The clock ride-over circuit as defined in claim 1 said output signal of the clock ride-over circuit is fed back to one input of said selector.

7. The clock ride-over circuit as defined in claim 2, wherein said clock detection unit comprises:

a differentiating unit of the first clock signal using the

second clock signal having a higher speed than the first clock signal, to output a differentiated clock signal of the first clock signal, which is used for generating a phase comparison signal supplied to said phase comparator.

8. A clock ride-over method in which an input digital signal synchronized with a first clock signal is converted into a digital signal synchronized with a second clock signal, and in which a result of conversion is output as an output digital signal, comprising:

(a) a first step of matching a phase of an input digital signal to a phase of said first clock signal to output said input digital signal phase-matched to said first clock signal;

(b) a second step of selecting said input digital signal phase-matched to said first clock signal or an output digital signal of the clock ride-over circuit, depending on a value of a selection signal of the same frequency as that of said first clock signal, to output a selected digital signal as an intermediate digital signal;

(c) a third step of synchronizing said intermediate digital signal to output said intermediate digital signal synchronized with said second clock signal as said output digital signal; and

(d) a fourth step of generating said selection signal based on said first clock signal and said second clock signal.

9. The clock ride-over method as defined in claim 8 wherein said fourth step comprises:

(d1) a step of detecting the phase of the first clock signal to output a detected result as a detection signal;

(d2) a step of outputting said selection signal by a self-running counter which uses said second clock signal as a clock signal; and

(d3) a step of comparing the phase of said detection signal to that of said selection signal to reset the phase of said self-running counter if the phase difference therebetween is outside an allowable range.

10. The clock ride-over method as defined in claim 9 wherein said allowable range begins with a timing at which said first clock signal changes and continues several periods of said second clock signal, said self-running counter outputting said selection signal at a trailing end of said allowable range after resetting.